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Technical Datasheet

takeMS TMS51B264C08x-534xx

Description

These Memory devices are JEDEC standard unbuffered DIMM modules, based on CMOS DDR2 SDRAM technology.
These devices consist of CMOS DDR2 SDRAMs in FBGA packages on a 240-pin glass epoxy substrate.The memory array is designed with Double Data Rate (DDR2) Synchronous DRAMs for unbuffered applications.
The pipelined, multibanked architecture of DDR2 SDRAMs allows for concurrent operation, thereby providing high, effective bandwidth.
Decoupling capacitors are mounted on the PCB board in parallel for each DDR2 SDRAM, which provides proper voltage supply impedance over the whole frequency range of operations, in accordance with JEDEC specifications.
These modules feature Serial Presence Detect (SPD) based on a serial EEPROM device, using the 2-pin I2C protocol.

Features
240-pin Unbuffered DDR2 SDRAM
JEDEC standard 1.8V I/O (SSTL_18-compatible)
Auto Refresh (CBR) and Self Refresh Mode
Off-Chip Driver (OCD) Impedance Adjustment
On-Die Termination (ODT) supports termination values of 50, 75, and 150 ohms
Serial Presence Detect (SPD) with EEPROM
Module layout is based on JEDEC standard routing guidelines
Impedance controlled 6-layer PCB Technology
JEDEC standard form factor (133.35 mm x 30.0 mm)
DQS edge-aligned with data for READs
DQS center-aligned with data for WRITEs
Operating Temperature 0°C ~ 75°C

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Technical details

- **512 MB longdimm module**
- **64Mx8 IC organisation**
- **x64 module organisation**
- **533MHz / PC2 4200**
- **single sided / 8 ICs**
- **CAS Latency 4 at max. memclock**

For pin configuration please check www.takems.com/support/index.php

If you have any questions regarding our products you can contact us via email: info@takems.com

Order-No.: **TMS51B264C08x-534xx**

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